Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VCC1**
2. **N. AOUT**
3. **AOUT**
4. **N. AIN**
5. **AIN**
6. **N. BOUT**
7. **BOUT**
8. **VEE**
9. **N. BIN**
10. **BIN**
11. **VBB**
12. **N. CIN**
13. **CIN**
14. **N. COUT**
15. **COUT**
16. **VCC2**

**.038”**

**2**

**3**

**4**

**5**

**1 16 15 14**

**6 7 8 9**

**13**

**12**

**11**

**10**

**.039”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: A**

**APPROVED BY: DK DIE SIZE .038” X .039” DATE: 5/24/21**

**MFG: ON SEMI THICKNESS .014” P/N: MC10H116**

**DG 10.1.2**

#### Rev B, 7/1